Reg. No. : | | | | | | | | | | |

R 3240

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Fourth Semester

(Regulation 2004)

Computer Science and Engineering

CS 1251 — COMPUTER ARCHITECTURE

(Common to Information Technology)

(Common to B.E. (Part-Time) — Third Semester — Regulation 2005)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. A memory byte location contains the pattern 00101100. What does this pattern represent when interpreted as a number? What does it represent as an ASCII Code?

2. What is the information conveyed by addressing modes?

3. Draw the full adder circuit using two half adders.

4. What are the various ways of representing signed integers in the system?

5. What are the advantages and disadvantages of hard wired and micro programmed control?

6. What is data hazard in pipelining? What are the solutions?

7. What is virtual memory? How is it implemented?

8. What will be the width of address and data buses for a 512 K $\times$ 8 memory chip?

9. Why do we need DMA?

10. What is the difference between subroutine and interrupt service routine?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain how the processor is interfaced with the memory with a neat block diagram and explain how they communicate. (10)

(ii) What do you know about bit, bytes, nibbles and word? What are big-endian and little-endian assignments of addresses? (6)

Or

(b) (i) Write notes on Instruction formats. (4)

(ii) List the various addressing modes. Give a brief explanation of each of them with an example. (8)

(iii) Describe the organization of a stack. (4)

12. (a) (i) Design a 4-bit carry-look ahead adder and explain its operation with an example. (8)

(ii) Design a binary multiplier using sequential adder. Explain its operation. (8)

Or

(b) (i) Write about the CSA method of fast multiplication. Prove how it is faster with an example. (8)

(ii) Draw the circuit for integer division and explain. (8)

13. (a) (i) Explain the Instruction cycle highlighting the sub-cycles and sequence of steps to be followed. (8)

(ii) Draw the single bus and three bus organization of the data path inside a processor. (4)

(iii) Describe the organization of micro programmed control unit. (4)

Or

(b) (i) Design a 4-stage instruction pipeline and show how its performance is improved over sequential execution. (8)

(ii) Highlight the solutions of Instruction hazards. (8)

14. (a) (i) Write notes on static memories. (8)

(ii) Explain the concept of memory hierarchy. (8)

Or

(b) Write notes on :

(i) ROM Technologies.

(ii) Memory Inter leaving.

(iii) Set associative mapping of cache.

(iv) RAID Disk arrays. (16)

15. (a) (i) Explain how I/O devices can be interfaced with a block diagram. (8)

(ii) How do you connect multiple I/O devices to a processor using interrupts? Explain with suitable diagrams. (8)

Or

(b) Write notes on :

(i) DMA.

(ii) Bus Arbitration.

(iii) Printer-Processor Communication.

(iv) USB. (16)
